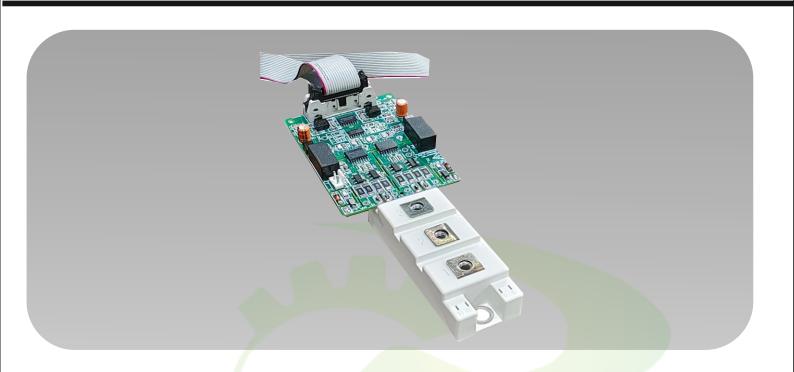


2 CHDIG_PRO_485_F10



FEATURES

- Optimized for use with 34 & 64 Half- Bridge Power Modules
- High-Frequency, Ultra-Fast Switching Operation
- Onboard 2 W Isolated Power Supplies
- Dead band settable
- Primary OVLO and Reverse Polarity Protection
- Differential Inputs for Increased Noise Immunity
- Increased over current trip level versatility
- Low Power dual channel driver 2X1 Watt Output Power
- Up to 2100V DC BUS
- Active shut down
- 4A Internal Active Miller clamp function
- 400-mA soft turn-off when fault happens
- 5.7 KV rms isolation
- Switching frequency up to 100 KHz
- Less than 130 ns propagation delay time
- Primary/Sec. Supply under voltage lockout
- Vce monitoring for short circuit protection
- 200 ns response time fast DESET protection
- Isolated analog sensor with PWM output for -
 - 1. Temperature sensing with NTC, PTC or thermal diode
 - 2. DC Bus bar voltage sensing

ADVANTAGES

- On board isolated DC-DC converter No need of separate SMPS.
- Interface for 3.3V...5 V logic level -Direct compatible with any Controller.
- Common fault feedback signal tointerface with controller Avoid Extra component.
- Field configurable blocking time -Flexibility in your hand, use any makeSIC.
- User Selectable Rg-on & off

APPLICATIONS

- Drives
- EV Charger/Battery Charger
- Converter Inverter
- UPS
- Solar Inverter
- Medical X-Ray

LED INDICATION

| 1. ERROR: High to Low (FLT) | |
|---|--|
| 2. Power supply monitoring High to Low. (Rdy) | |

Power ON: Green (Normally OFF, ON during Power supply fault)

ERROR: RED (ON during Under Voltage / DESAT/ IGBT Fault)

Dead Band Tunning

| C2 & C3 | DEAD BAND TIME (uSec) |
|---------|-----------------------|
| 47PF | 1 |
| 100PF | 3 |
| 220PF | 6 |
| 330PF | 7 |

| Parameter | Symbol | Min. | Typ · | Max. | Unit | Test Conditions |
|--|-----------------|-------|----------|-------|-------|---|
| Supply Voltage | VDC | 14.25 | 15 | 15.75 | | |
| Secondary Under Voltage Lockout | VUVLO | | 13. 5 | | | |
| Secondary UVLO Hysteresis | VHYS | | 0.0 6 | | V | |
| Over Voltage Clamping | Vovlo | 18 | 20 | 22 | | |
| High Level Logic Input Voltage | VIH | 3.5 | | 5.5 | | |
| Low Level Logic Input Voltage | VIL | 0 | | 1.5 | | Single-Ended Inputs |
| Differential Input Common Mode Range | VIDCM | - | ±2.5 | ±7 | | Differential Inputs |
| Positive-going input threshold voltage, differential input | VIT+ | | | 0.2 | V | VID=VPos-Line-VNeg-Line |
| Negative-going input threshold voltage, differential input | VIT- | -0.2 | | | | VID-VF05-Lille Viveg-Lille |
| Differential Output Magnitude | VOD | 2 | 3.7 | | | RL=100Ω |
| High level Output Voltage | VGATE,HIG H | | +15 | | V | |
| Low level Output Voltage | VGATE,LO W | | -5 | | | |
| Working Isolation Voltage | VIOWM | | 210 0 | | | VRMS |
| Isolation Capacitance | VISO | | 4.9 | | pF | Per Channel |
| Common Mode Transient Immunity | CMTI | 100 | | | kV/μs | VCM=1500V |
| Output Resistance ¹ | RG(IC)- ON | | 0.4 8 | 0.98 | | Gate Driver Buffer Tested at |
| | RG(IC)- OFF | | 0.4 7 | 0.81 | Ω 1Α | |
| External Turn-On Resistance ² | RG(EXT)- ON | | 1 | | | ExternalSMDResistor25 12(6432Metric) |
| External Turn-Off Resistance ² | RG(EXT)- OFF | | 1 | | | |
| Output Rise Time | ton | | 223 | | | RG(EXT)=1Ω,CLOAD=47nF |
| Output Fall Time | tOFF | | 208 | | | From10%to90% |
| Propagation Delay(Turn-Off) | tPHL | | 120 | | ns | RG(EXT)=1Ω,CLOAD=0nF |
| Propagation Delay(Turn-On) | tPHL | | 125 | | | From50%to50% |
| Over-current Blanking Time | tBla nk | | 600 | | | RG(EXT)=1Ω,CLOAD=47nF |
| Over-current Propagation Delay to FAULT Signal Low | tpD- FAULT | | 1.3 | | μs | Does Not Include Blanking |
| Soft-Shutdown Time | tss | | 1.3 | | | RG(EXT)=1Ω,CLOAD=47nF |
| Soft-Shutdown Resistance ³ | RSS | | 5 | | | Tested at 25mA |
| Miller Clamp Resistance | RMC | | 1.1 | 2.75 | Ω | Tested at 100mA |

| Pin Number | Parameter | Description |
|------------|-------------|---|
| 1 | $V_{	t DC}$ | Power supply input pin(+15V Nominal Input) |
| 2 | Common | Common |
| 3 | HS_P_PWM | Positive line of 5V differential high-side PWM signals pair. Terminated into 120Ω |
| 4 | HS_N_PWM | Negative line of 5V differential high-side PWM signal pair. Terminated into 120Ω |
| 5 | LS_P_PWM | Positive line of 5V differential low-side PWM signals pair. Terminated into 120Ω |
| 6 | LS_N_PWM | Negative line of 5V differential low-side PWM signal pair. Terminated into 120Ω |
| 7 | FAULT-P(*) | Positive line of 5V differential fault condition signal pair. Drive strength 20mA.A low state on FAULT indicates when a desaturation & power supply fault has occurred. The presence of a fault precludes the gate drive output from going high. |
| 8 | FAULT-N(*) | Negative line of 5V differential fault condition signal pair. Drive strength 20mA. |
| 9 | RTD_P | Positive line of 5V differential fault condition signal pair. Drive strength 20mA |
| 10 | RTD_N | Negative line of 5V differential fault condition signal pair .Drive strength20mA. |
| 11 | NC | Unused, do not connect |
| 12 | Common | Common |
| 13 | PWM-EN | Pull down to disable PWM input logic. Pull up or leave floating to enable. Gate driver output will be held low through turn-off gate resistor if power supplies are enabled. |
| 14 | Common | Common |
| 15 | Reset | When a fault exists, bring this pin high 5V to clear the fault. |
| 16 | Common | Common |

^{*} Inputs3-8aredifferentdifferentialpair

SHORT CIRCUIT PROTECTION

| VCE MONITORING THRESHOLD |
|--------------------------|
| AVAILABLE RESPONSE TIME |
| MINIMUM RESPONSE TIME |
| MINIMUN BLOCKING TIME |

| 9.2 V (Internally fix) |
|--------------------------|
| 1 μSec (User selectable) |
| 1.0 μSec |
| 1.0 μSec |

LOGICAL INPUTS & OUTPUTS

| Interface Logic level | : 3 .3 to 5.0 V | | |
|--|--------------------|--|--|
| Fault output for Deset and Power supply failure | | | |
| External Reset | | | |
| Enable | | | |
| RTD_Output (Isolo temperature Read device) | | | |

| 3.3 TO 5.0 V |
|--------------------------------------|
| Active Low (0V) for Fault and Normal |
| for Active High (5v) |
| Reset by active high (5V) |
| Before use external reset please |
| remove R48 & 49 mention in driver at |
| bottom side. |
| By default auto reset available |
| Active high (5V) when normal else |
| active low Enable and both PWM |
| disable |
| 0.6 to 1.6V(25° to 135°C) |

TIMING CHARACTERISTIC

| TURN ON DELAY-T |
|----------------------------|
| TURN OFF DELAY-T |
| OUTPUT RISE TIME T |
| OUTPUT FALL TIME T |
| TRANSMISSON DELAY OF FAULT |

| 185 ns | |
|-----------|--|
| 185 ns | |
| 35 ns MAX | |
| 35 ns MAX | |
| 330 ns | |

| PROTECTION AVAILABLE ON DRIVER MODE |
|---|
| Primary/Secondary Under voltage monitoring. |
| Power supply short circuit & reverse polarity protection. |
| Vce monitoring for circuit protection |
| Schmitt trigger at the Input stage, highly susceptible to noise |
| Interlocking when both pulse high |
| Soft Shut down for Over Voltage Protection |

| OUTPUT VOLTAGE / CURRENT / POWER | | | |
|----------------------------------|----------------------------------|--|--|
| TURN ON VOLTAGE , V | 14.5 - 15.5V, any load condition | | |
| TURN OFF VOLTAGE , V | -4 to – 5.5V, No load | | |
| GATE PEAK CURRENT lout | +15 A source -15 A sink | | |
| INTERNAL GATE RESISTANCE | 0.0Ω | | |
| EXTERNAL GATE RESISTANCE | 1.5 Ω-10 Ω | | |
| SWITCHING FREQUENCY, F | 100Khz | | |
| OUTPUT POWER | 2.4 W @105°C | | |
| GATE AVERAGE CURRENT lavg | 100ma | | |

| ELECTRICAL ISOLATION | | |
|-----------------------------|--------|--|
| Test Voltage (50HZ/60SEC) | | |
| Primary to Secondary side | 5.7 KV | |
| Secondary to Secondary side | 5.7 KV | |

| MECHANICAL DIMENSION (OPTION 2) | | |
|---------------------------------|----------------------------|--|
| РСВ | 85 X 65 mm | |
| Mounting Hole | 53.5 X 28.5 X 2 mm | |
| Panel Mounted | Direct SIC module mounting | |
| Enclosure | Open Frame | |
| Weight | 0.3 Kg | |
| Layer | 4 Layer | |

| ENVIRONMENTAL TEMPERATURE | | |
|---------------------------|---------------|--|
| Working temperature | -40 to 105 ºC | |
| Storage temperature | -40 to 90 ºC | |

All usual SIC-MOSFET up to 400A /1700V.

Driving power depends on switching frequency so in case of any doubt during selection process please contact us.

MODULE LAYOUT

